University of Saskatch
Department of Electrical E
EE 232 – Digital Electronics
Final Examination

Instructor: Seok-Bum Ko April 17, 2003
Duration: 2 hours

1. The addition and subtraction operations can be combined into one circuit with one common binary full adder. Please provide the logic diagram of a 4-bit adder-subtractor circuit and explain the detailed operation. (10 points)
Hint: Use the control signal, *S* and exclusive-OR gate(s).

2. Draw the diagram using J-K flip-flops and provide the waveform for a MOD-16 down counter. (10 points)

3. It is desired to combine several $2K \times 8$ PROMs to produce a total capacity of $32K \times 8$. How many PROM chip(s) are needed? How many address lines are required? What size decoder would be need? Describe what address lines are used? (10 points)

4. Please simplify the expression, $y = \overline{(C+D)} + \overline{A}C\overline{D} + A\overline{B}\overline{C} + \overline{A}\overline{B}CD + AC\overline{D}$ using a K-map? (10 points)

5. Design a BCD-to-Excess-3 code converter. The excess-3 code for a decimal digit is the binary combination corresponding to the decimal digit plus 3. You should provide the truth table, K-Map(s) and the logic diagram. (10 points)

The End

BCD → O + 3